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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,610	12/29/2000	William A. Harris	H16-26054 US	8597

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HONEYWELL INTERNATIONAL INC.
101 COLUMBIA ROAD
P O BOX 2245
MORRISTOWN, NJ 07962-2245

EXAMINER
COX, CASSANDRA F

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,610	HARRIS, WILLIAM A.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,6-9,20 and 21* is/are allowed.

6)☒ Claim(s) *4-5,11-13 and 15-17* is/are rejected.

7)☒ Claim(s) *14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *04 March 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

2. Claims 4-5, 11-13 and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Li et al. (U.S. Patent No. 5,058,132).

In reference to claim 11, Li discloses in Figure 2, a circuit (100) for generating multiphase clock signals, the circuit comprising: a clock generator (the clock generator is seen to be the oscillator 120; column 4, line 65 - column 5, line 15) for generating a first clock at a clock frequency F_0; a phase lock loop circuit (102) receiving the first clock signal (116) and providing an output signal (124); and a Johnson counter (114) having N stages connected to receive as an input the output signal (124) of the phase lock loop circuit (102) and providing an output signal (LBC1-5) as an error signal to the phase lock loop circuit (column 5, lines 25-28); the Johnson counter (114) also connected for providing output signals (LBC1-LBC5) from each of the N stages of the Johnson counter (114) as further clock signals. The same applies to claims 4-5, wherein the multistage counting circuit is seen to be the Johnson counter (114) and the clock generator is seen to be the oscillator (120; column 4, line 65- column 5, line 15).

In reference to claim 12, the output signal of the phase lock loop circuit has a frequency of $2NF_0$.

In reference to claim 13, Li discloses in Figure 2, a circuit for receiving an input clock signal (116) and generating a plurality of clock signals (LBC1-LBC5) having

frequencies identical to the input clock signal (116) and predetermined phase displacements from the input signal, comprising: a phase detector (104) for comparing an input clock signal (116) to a feedback signal (123) and providing an output signal (121) corresponding to the phase difference between the input clock signal (116) and the feedback signal (123); a low pass filter and gain stage (106) receiving the output signal from the phase comparator (104) and producing a control signal (125); a voltage controlled oscillator (108) for receiving the control signal and producing an oscillator output signal (124) having a frequency corresponding to the control signal (125); and a multistage counting circuit (114) connected to receive the oscillator output signal (124) and provide the feedback signal (123; column 5, lines 50-67) to the phase detector (104) and a plurality of clock signals (LBC1-LBC5) at the frequency of the input clock signal (116) and phase shifted from the clock signal. The same applies to claim 16.

In reference to claim 15, Li also discloses in Figure 2 that the multistage counting circuit (114) is a Johnson counter having N stages.

In reference to claim 17, Li also discloses in column 5, lines 1-22 that the frequency (125MHz) of the voltage controlled oscillator output signal (124) is a multiple of the frequency (12.5 MHz) of the input clock signal (116).

3. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Fujii (U.S. Patent No. 5,315,269).

In reference to claim 11, Fujii discloses in Figure 5, a circuit for generating multiphase clock signals, the circuit comprising: a clock generator (104) for generating a first clock at a clock frequency F_0; a phase lock loop circuit (101, 102, 103) receiving the

first clock signal (output of 104) and providing an output signal (OUT); and a Johnson counter (105; see column 5, lines 1-2 and 14-16) having N stages connected to receive as an input the output signal (OUT) of the phase lock loop circuit (101, 102, 103) and providing an output signal as an error signal to the phase lock loop circuit (column 3, lines 60-63); the Johnson counter (105) also connected for providing output signals (shown in Figure 8) from each of the N stages of the Johnson counter (105) as further clock signals.

Response to Arguments

4. In response to applicant's argument with respect to claim 13, that the Li reference fails to show the plurality of clock signals "phase shifted from the clock signal", this argument is not persuasive because the "time-delayed" signals in LI are inherently phase shifted from each other, i.e., it is well-known in the art that time-delaying and phase shifting are synonymous.

In response to applicant's argument that claim 4 has been amended to recite that the output signals from the counter each have a phase "displaced from the phase of the input signal by a fixed angle", it is noted that the amendment filed on 3/04/02 failed to amend the claim, and therefore the rejection has been repeated.

In response to applicant's argument that claims 11 and 12 have been canceled, it is noted that the amendment filed on 3/04/02 failed to cancel those claims, and therefore the rejection has been repeated.

Allowable Subject Matt r

5. Claims 1-3, 6-9 and 20-21 are allowed.

6. Claims 14 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claims 14 and 19 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the plurality of clock signals are shifted from each other by fixed angular increments in combination with the rest of the limitations of the base claims and any intervening claims.

8. The following is an examiner's statement of reasons for allowance: Claims 1-3 and 20-21 are allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the clock signals each have a phase displaced from the phase of the other by 360°/2N in combination with the rest of the limitations of the base claims and any intervening claims. Claims 6-9 are allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the plurality of clock signals are shifted from each other by fixed angular increments in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

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June 3, 2002

Kenneth B. Wells
Primary Examiner